REMARKS

Claims 1-4 and 16-23 are all the claims presently being examined in the application. Based on a telephone interview with the Examiner on April 25, 2003, in which the invention and the prior art were discussed, the Examiner indicated that the amendments to independent claims 1, 4, and 20 would overcome the currently cited references. New Claims 21-23 have been added. Claims 1-4 and 16-20 stand rejected on prior art grounds.

Claims 1 and 3 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the acknowledged prior art of Fig. 1 in view of Song, et al. (U.S. Patent No. 6,197,615 B1). Claims 2 and 16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the acknowledged prior art of Fig. 1 in view of Song, et al. and further in view of Enomoto, et al. (U.S. Patent No. 5,055,321). Claim 17 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over acknowledged prior art of Fig. 1 in view of Song, et al. and further in view of Kaskoun, et al. (U.S. Patent No. 5,816,478). Claims 4, 18, and 19 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kweon, et al. (U.S. Patent No. 5,834,832) in view of Sato, et al. (U.S. Patent No. 5,519,251). Claim 20 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over the acknowledged prior art of Fig. 1 in view of Lee (U.S. Patent No. 5,872,399).

It is noted that the amendments are made only to more particularly define the invention and not for distinguishing the invention over the prior art, for narrowing the scope of the claims, or for any reason related to a statutory requirement for patentability.

It is further noted that, notwithstanding any claim amendments made herein, Applicant's intent is to encompass equivalents of all claim elements, even if amended herein or later during prosecution.

I. THE CLAIMED INVENTION

Applicant's invention, as disclosed and claimed, for example by independent claim 1, is directed to a semiconductor device.

The semiconductor device includes a semiconductor chip, a chip-mounting substrate which is provided with the semiconductor chip mounted on a top surface thereof and first conductive pads formed on a bottom surface thereof and connected with the semiconductor chip electrically, solder balls formed on the first conductive pads, a printed circuit board on which second conductive pads connected with the solder balls are formed, a solder mask formed on a bottom surface of the chip-mounting substrate, the solder mask having an uneven roughness, and underfill material injected into a clearance formed between the chip-mounting substrate and the printed circuit board. The uneven roughness is formed on a surface which is brought into contact with the material of the printed circuit board. The uneven roughness exists on the bottom surface of the chip-mounting substrate. The uneven roughness on the bottom surface increases an area of a contact surface between the chip-mounting substrate and an underfill material. (See Page 15, lines 1-6; Page 16, lines 13-20; and Figures 2-4).

A second embodiment, as disclosed and claimed, for example by independent claim 20, is also directed to a semiconductor device. The semiconductor device includes an uneven roughness formed on a contact surface of the Cu wiring between the Cu wirings of the chip-mounting substrate and the solder balls. Specifically, the uneven roughness exists on a bottom surface of the Cu wirings with the Cu wirings being directly connected to the solder balls to form a joined surface. (See Page 19, lines 1-4 and lines 15-24; and Figures 5 and 6).

A third embodiment, as disclosed and claimed, for example by independent claim 4, is also directed to a semiconductor device. The semiconductor device includes a semiconductor chip, a lead frame which is provided with the semiconductor chip mounted

thereon and electrically connected with the semiconductor chip, and a printed circuit board including conductive pads which are formed thereon and brought into direct contact with a bottom surface of the lead frame. The uneven roughness exists on the bottom surface of the lead frame and a surface of the conductive pads. (See Page 20, lines 10-25; and Page 21, lines 18-28; Page 22, lines 6-11; and Figures 9A and 9B).

Conventional semiconductor devices do not have an uneven roughness formed on a bottom surface of a chip-mounting substrate or a pad situated between the solder ball and the insulating substrate. However, this configuration tends to decrease in reliability because a reduction occurs in the adhesive strength of an underfill material due to contamination or external mechanical stresses thus causing the underfill material to exfoliate from the chip-mounting substrate or the printed circuit board. (See Page 1, line 22 - Page 2, line 24; and Figure 1).

An aspect of the present invention includes a solder mask (sealing material) formed on a bottom surface of the chip-mounting substrate, the solder mask having an uneven roughness. This configuration through the use of the solder mask "seals the lands and the Cu wirings airtightly and the surfaces thereof can be made rough easily," promotes greater adhesive strength among the chip-mounting substrate, the underfill material and the printed circuit board (according to claim 1). (See Page 4, line 17 through Page 5, line 4; Page 15, lines 1-6 and lines 23-28; Page 16, lines 13-20; and Figures 2-4).

A similar feature in the second embodiment of a semiconductor device, as disclosed and claimed, for example by independent claim 20, includes the uneven roughness existing on a bottom surface of the Cu wirings with the Cu wirings being directly connected to the solder balls to form a joined surface, which increases greater adhesive strength between the Cu wirings and the solder balls. (See Page 19, lines 1-4; and lines 15-24; Page 20, lines 10-

25; and Page 21, lines 18-28; and Figures 5 and 6).

A similar feature in the third embodiment of a semiconductor device, as disclosed and claimed, for example by independent claim 4, includes an even roughness existing on a bottom surface of the lead frame and the surface of the conductive pads, which increases greater adhesive strength between the lead frame and the printed circuit board. (See Page 20, lines 10-25; and Page 21, lines 18-28; Page 22, lines 6-18; and Figures 9A and 9B).

As a result of these features, the semiconductor device experiences less internal exfoliation of the components, and thus operates with a high level of reliability. (See Page 3, lines 15-21; and Page 22, lines 17-18).

II. THE PRIOR ART REJECTION

A. The § 103(a) Rejection of Claims 1 and 3

First, the references, separately, or in combination, fail to teach, disclose or provide a motivation for being combined. In particular, the Prior Art pertains to semiconductor chips, which are attached to printed circuit boards, not to producing printed circuit boards. The Prior Art also does not disclose, teach or suggest improving surface bonding. (See Column 2, lines 39-48; and Page 2, line 25 through Page 3, line 21).

The Prior Art discloses a semiconductor device, which includes a printed circuit board and a semiconductor chip mounting substrate with an underfill material but without an uneven roughness existing on a bottom surface of a chip-mounting substrate or a pad situated between the solder ball and the insulating substrate. The Prior Art is specifically directed to solving a problem of the different thermal expansion coefficients between the printed circuit board and the chip mounting substrate by providing for an underfill material to absorb a stress

caused by these expansions. (See Page 1, line 22- Page 2, line 25). However, the Prior Art devices have decreased reliability because a reduction occurs in the adhesive strength of an underfill material due to contamination or external mechanical stresses thus causing the underfill material to exfoliate from the chip-mounting substrate or the printed circuit board. (See Page 1, line 22 - Page 2, line 24; and Figure 1).

By contrast, Song, et al. ("Song") does not have the same aim as the Prior Art.

Song discloses a method for producing a lead frame with "irregular dimples on their respective upper and lower surfaces." Song is specifically directed to solving debonding failures of the components while reducing the number of dimples on the surfaces of the inner leads, tie bars and die pad as the semiconductor device package is decreased in size. Accordingly, Song attempts to "improve the bonding strength between the lead frame and the molding compound as well as between the die pad and a semiconductor device." (See Song at Abstract; Column 1, lines 5-30 and lines 41-57; and Column 2, lines 1-29).

Nothing within Song, which focuses on bonding strength, has anything to do with underfill material for differences in thermal coefficients of expansion as disclosed in the Prior Art. Thus, the Prior Art teaches away from being combined with another invention, such as, Song.

Therefore, one of ordinary skill in the art would not have combined these references, absent hindsight. It is clear that the Examiner has simply read Applicant's specification and conducted a keyword search to yield the Prior Art and Song. Further, the Examiner provides no motivation or reason to combine other than to assert that it would have been obvious to one having ordinary skill in the art at the time to modify the Prior Art with Song to enhance bonding strength. Such an assertion does not take into account the distinct structural differences of the Prior Art and Song as indicated above, and further discussed below. Thus,

the Examiner's assertion attempts to solve a potential problem which does not ever exist with either the Prior Art or Song, and this assertion is clear proof of the Examiner's use of impermissible hindsight.

Second, even if combined, the references do not teach or suggest the features of independent claim 1. Specifically, there is no teaching or suggestion of at least a solder mask formed on a bottom surface of the chip-mounting substrate, the solder mask having an uneven roughness.

Song does not make up for the deficiencies of the Prior Art. Instead, Figure 3 of Song discloses a lead frame with "irregular dimples on their respective upper and lower surfaces." "[D]imples of the lead frame according to the present invention are irregular and are randomly formed throughout the entire surface of the die pad (i.e., upper and lower surfaces)." The dimples "increase the surface area and thus the bonding strength between die pad and device, and between die pad and molding compound." (See Column 3, line 35 - Column 4, line 21; and Figure 3). Thus, Song teaches that the dimples are directly formed on the die pad without any solder mask, or similar layer, formed on the die pad.

In contrast, Applicant's invention discloses including a solder mask formed on a bottom surface of the chip-mounting substrate, the solder mask having an uneven roughness. In particular, the solder mask may be formed over the insulating substrate, the land and the copper wiring and the roughness is formed in the solder mask. As explained in the Application, the solder mask "seals the lands and the Cu wirings airtightly and the surfaces thereof can be made rough easily," promoting greater adhesive strength among the chip-mounting substrate, the underfill material and the printed circuit board (according to claim 1). (See Page 4, line 17 through Page 5, line 4; Page 15, lines 1-6 and lines 23-28; Page 16, lines 13-20; and Figures 2-4).

As indicated, Song does not disclose any type of solder mask, or similar layer, let alone the solder mask having an uneven roughness. Indeed, Song forms the dimples directly on the die pad, not on a solder mask situated on the substrate to achieve the advantages of Applicant's invention.

Therefore, neither the Prior Art nor Song teaches or suggests a solder mask formed on a bottom surface of the chip-mounting substrate, the solder mask having an uneven roughness as recited in claim 1.

For at least the reasons outlined above, Applicant respectfully submits that neither the Prior Art nor Song disclose, teach or suggest all of the features of the independent claim 1, and dependent claims 2, 3, 16, and 17. Additionally, the dependent claims are patentable not only by virtue of their dependency from the respective independent claim 1, but also by the additional limitations they recite.

B. The Enomoto Reference

Regarding claims 2 and 16, to make up for the deficiencies of the Prior Art and Song discussed above, the Examiner relies on Enomoto, et al. ("Enomoto"). Enomoto fails to do so.

First, Enomoto does not have the same aim as either the Prior Art or Song as discussed above, and the urged combination would not have been made, absent hindsight.

Enomoto's discloses an adhesive for electroless plating formed by dispersion of heat-resistant granules soluble in a heat resistant resin. (See Enomoto at Abstract). Enomoto is specifically directed to solving the drawbacks in the adhesive for electroless plating in producing the printed circuit boards (PCBs). Indeed, Enomoto attempts to increase the adhesion property between a PCB and the patterns thereon. (See Column 1, lines 5-15; and

Column 2, lines 38-48).

Nothing within Enomoto, which focuses on adhesives for electroless plating, has anything to do with underfill material for differences in thermal coefficients of expansion as disclosed in the Prior Art. Thus, the Prior Art teaches away from being combined with another invention, such as, Enomoto.

Similarly, nothing within Enomoto has anything to do with solving debonding failures of the components while reducing the number of dimples on the surfaces of the inner leads, tie bars and die pad as the semiconductor device package is decreased in size as disclosed in Song. Thus, the Prior Art and Song teach away from being combined with each other as well another invention, such as, Enomoto.

Therefore, one of ordinary skill in the art would not have combined these references, absent hindsight.

Secondly, Enomoto does not disclose, teach or suggest including a solder mask formed on a bottom surface of the chip-mounting substrate, the solder mask having an uneven roughness as recited in claim 1.

Further, Enomoto does not disclose, teach or suggest including where the uneven roughness is formed on at least one of the first conductive pads and the second conductive pads as recited in claim 2 of the invention. Further, Enomoto does not disclose, teach or suggest including the printed circuit board has a dimple-like shaped configuration as recited in claim 16.

Instead, Enomoto recites an adhesive for electroless plating formed by dispersion of heat-resistant granules soluble in a heat resistant resin. (See Enomoto at Abstract; and Figure 1). Since the Examiner previously admitted that Enomoto do not disclose, teach or suggest "the uneven roughness existing on a bottom surface of the chip-mounting substrate,"

Enomoto is deficient and thus does not teach the specific limitations of dependent claims 2 and 16. (See Office Action, October 21, 2002, Page 5, Section 10).

For the reasons stated above, the claimed invention, defined by dependent claims 2 and 16, is fully patentable over the cited references.

C. The Kaskoun Reference

Regarding claim 17, to make up for the deficiencies of the Prior Art and Song, the Examiner relies on Kaskoun, et al. ("Kaskoun"). Kaskoun fails to do so.

First, Kaskoun discloses a method of flip-chip bonding of two electronic components without the use of a flux material. (See Kaskoun at Abstract).

Kaskoun is specifically directed to solving the drawbacks in the soldering process of semiconductor device in assembling at least two electronic components. Indeed, Kaskoun attempts to eliminate "the risks of deforming the solder balls, and does not add appreciable complexity or cost to the manufacturing process." (See Column 1, lines 5-20 and 50-63; and Column 2, lines 29-57).

Nothing within Kaskoun, which focuses on flip-chip bonding without the use of a flux material, has anything to do with underfill material for differences in thermal coefficients of expansion as disclosed in the Prior Art. Thus, the Prior Art teaches away from being combined with another invention, such as, Kaskoun.

Similarly, nothing within Kaskoun has anything to do with solving debonding failures of the components while reducing the number of dimples on the surfaces of the inner leads, tie bards and die pad as the semiconductor device package is decreased in size as disclosed in Song. Thus, the Prior Art and Song teach away from being combined with each other as well another invention, such as, Kaskoun.

Therefore, one of ordinary skill in the art would not have combined these references, absent hindsight.

Secondly, Kaskoun does not disclose, teach or suggest including a solder mask formed on a bottom surface of the chip-mounting substrate, the solder mask having an uneven roughness as recited in claim 1.

Further, Kaskoun does not disclose, teach or suggest including the chip-mounting substrate has a slit-like shaped configuration as recited in claim 17.

Instead, Kaskoun recites a method of flip-chip bonding without the use of a flux material. (See Kaskoun at Abstract; and Figure 1). Since Kaskoun do not disclose, teach or suggest a solder mask, let alone, a solder mask formed on a bottom surface of the chip-mounting substrate, the solder mask having an uneven roughness, Kaskoun is deficient and thus does not teach the specific limitations of dependent claim 17.

For the reasons stated above, dependent claim 17 is fully patentable over the cited references.

D. The § 103(a) Rejection of Claims 4, 18 and 19

First, the references, separately, or in combination, fail to teach, disclose or provide a motivation for being combined. In particular, Kweon, et al. ("Kweon") pertains to a packaging structure for a surface mounting type semiconductor package with at least one semiconductor chip mounted on a die pad where a conductive pattern is formed on a printed circuit board located beneath an exposed side of a die pad of the package (See Kweon at Abstract; and Column 1, lines 10-23).

Kweon is specifically directed to "improving the grounding property by the particular packaging structure, which allows a reduction of the noise, without deteriorating the operation speed or mounting density of the package" by providing "a nonconductive thin film

as a capacitor formed in a space between the die pad and the conductive pattern where the space has a voltage difference." (See Column 3, lines 8-33).

By contrast, Sato, et al. ("Sato") does not have the same aim as Kweon.

Sato discloses a semiconductor device with "a portion of leads exposed at a bottom surface of a package so as to improve the package density of the semiconductor device." Sato is specifically directed to improving the packaging density of semiconductor devices as surface mounting connects the leads at the surface of the substrate. Accordingly, Sato attempts to reduce the size of the semiconductor devices using simple processes." (See Song at Abstract; Column 1, lines 5-25; Column 2, lines 30-55; and Column 3, lines 1-12).

Nothing within Sato, which focuses on improving packaging density has anything to do with "improving the grounding property by the particular packaging structure" as disclosed in Kweon. Thus, the Kweon teaches away from being combined with another invention, such as, Sato.

Therefore, one of ordinary skill in the art would not have combined these references, absent hindsight. It is clear that the Examiner has simply read Applicant's specification and conducted a keyword search to yield Kweon and Sato. Further, the Examiner provides no motivation or reason to combine other than to assert that it would have been obvious to one having ordinary skill in the art at the time to use the uneven rough contact surfaces of Sato in Kweon to increase the strength of the external terminal.

Second, even if combined, the references do not teach or suggest the features of independent claim 4. Specifically, there is no teaching or suggestion of a printed circuit board including conductive pads which are formed thereon and brought into direct contact with a bottom surface of the lead frame, and uneven roughness existing on the bottom surface of the lead frame and the surface of the conductive pads. (See Page 20, lines 10-25; and Page

21, lines 18-28; Page 22, lines 6-11; and Figures 9A and 9B).

Sato does not make up for the deficiencies of Kweon. Instead, Figures 7A, 14C, and 16A, of Sato disclose a conventional a semiconductor device with "a portion of leads exposed at a bottom surface of a package." The leads have an external terminal with a bottom surface and "at least some of the leads ha[ve] dimples formed thereon." Further, a conductive adhesive agent is provided between the external terminal of the lead and an electrode pad. The electrode pad is formed on the circuit substrate. (See Column 5, lines 43-61; Column 9, lines Column, 10 lines 14-47; and Figures 7A, 14C and 16A). Thus, Sato teaches that the dimples are only formed on the bottom surface of the lead frame, not the surface of the conductive pads as in claim 4.

In contrast, Applicant's invention discloses including a printed circuit board including conductive pads which are formed thereon and brought into direct contact with a bottom surface of the lead frame, and uneven roughness exists on the bottom surface of the lead frame and the surface of the conductive pads.

Further, in particular, the lead of the lead frame has a roughness, for example as recited in new claim 24, and further the bottom surface of the lead may have the roughness. Since the uneven roughness is formed on the lead frame and the conductive pads, this configuration provides for greater adhesive strength between the lead frame and the printed circuit board. (See Page 20, lines 10-25; and Page 21, lines 18-28; Page 22, lines 6-18; and Figures 9A and 9B).

As indicated, Sato forms the dimples only on the bottom surface of the lead frame whereas in the invention the uneven roughness exists on the bottom surface of the lead frame and the surface of the conductive pads where the printed circuit board includes the conductive pads. As a result of the uneven roughness existing only on the bottom surface of the lead

frame in Sato, this configuration may result in reduced adhesion between the lead frame and the printed circuit board when compared to Applicant's invention.

Therefore, neither Kweon nor Sato teaches or suggests a printed circuit board including conductive pads which are formed thereon and brought into direct contact with a bottom surface of the lead frame, and uneven roughness exists on the bottom surface of the lead frame and the surface of the conductive pad as recited in independent claim 4. The invention provides for greater adhesive strength between the lead frame and the printed circuit board, and thus the semiconductor device experiences less internal exfoliation of the components and operates with a high level of reliability. (See Page 3, lines 15-21; Page 20, lines 10-25; and Page 21, lines 18-28; Page 22, lines 6-18; and Figures 9A and 9B).

For at least the reasons outlined above, Applicant respectfully submits that neither Kweon nor Sato disclose, teach or suggest all of the features of the independent claim 4, and dependent claims 18 and 19. The dependent claims are patentable not only by virtue of their dependency from the respective independent claim 4, but also by the additional limitations they recite.

E. The § 103(a) Rejection of Claim 20

First, the references, separately, or in combination, fail to teach, disclose or provide a motivation for being combined.

Lee ("Lee") does not have the same aim as the Prior Art. Lee discloses a solder ball land metal structure of a ball grid array semiconductor package. Lee is specifically directed to solving separation of the solder balls from the land metal elements which prevents a ball grid array semiconductor package from functioning. Accordingly, Lee attempts to obtain "a maximum contact area between a solder ball land metal element ... and a solder ball fused on the land metal element." (See Lee at Abstract; Column 1, lines 5-35; Column 2, lines 50-65;

and Column 3, lines 10-20).

Nothing within Lee, which focuses on maximizing the bonding area of a solder ball, has anything to do with underfill material for differences in thermal coefficients of expansion as disclosed in the Prior Art. Thus, the Prior Art teaches away from being combined with another invention, such as, Lee.

Therefore, one of ordinary skill in the art would not have combined these references, absent hindsight.

Second, even if combined, the references do not teach or suggest the features of independent claim 20. Specifically, there is no teaching or suggestion of at least one feature, including the uneven roughness exists on a bottom surface of the Cu wirings, and the Cu wirings are directly connected to the solder balls to form a joined surface.

Lee does not make up for the deficiencies of the Prior Art. Instead, Figure 5E of Lee discloses a solder ball land metal structure of a ball grid array semiconductor package. Solder balls are formed over a gold film, which is plated over a nickel film. The nickel film is plated over the copper land metal element, which is situated over a chip mounting substrate. An etching hole may be formed through the land metal element to increase the contact area between the solder ball and the land metal element. Accordingly, "the solder ball is fused on the nickel film." (See Column 2, lines 9-32; Column 4, lines 1-30; Column 5, lines 1-25; and Figures 3 and 5). Thus, Lee teaches that the solder balls are indirectly formed on the land metal structure.

In contrast, Applicant's invention discloses including the uneven roughness exists on a bottom surface of the Cu wirings, and the Cu wirings are directly connected to the solder balls to form a joined surface. In particular, the "solder balls are connected with the Cu wirings by thermal compression welding, where the surfaces of the Cu wirings have been

made rough beforehand" eliminating the need for additional solder type layers of nickel and gold like Lee's conventional structure. (See Page 19, lines 1-5; and Figures 5 and 6). Thus, this configuration increases adhesive strength between the Cu wirings and the solder balls compared to conventional structures using indirect bonding of the components. (See Page 19, lines 1-4; and lines 15-24; Page 20, lines 10-25; and Page 21, lines 18-28; and Figures 5 and 6).

As indicated, Lee bonds the solder ball to the land metal structure through the use of intermediately situated nickel and gold layers, whereas Applicant's invention directly connects the Cu wirings to the solder balls without any additional layer, e.g., a nickel or gold intermediate layer. In addition to the structural differences, Lee would likely not function to form as great an adhesive strength between the solder ball and the land metal structure when compared to Applicant's invention. Accordingly, Lee does not disclose, teach or suggest including at least one feature of Applicant's invention, including the uneven roughness exists on a bottom surface of the Cu wirings, and the Cu wirings are directly connected to the solder balls to form a joined surface.

Finally, in Lee, only several etching holes are formed in the copper land metal structure whereas Applicant's invention teaches continuous roughness on the bottom surface of the copper wiring, for example as recited in new claim 27. Thus, Applicant's invention provides for greater adhesive strength between the Cu wirings and the solder balls when compared to Lee's conventional structure.

Therefore, neither the Prior Art nor Lee teaches or suggests the uneven roughness exists on a bottom surface of the Cu wirings, and the Cu wirings are directly connected to the solder balls to form a joined surface as recited in claim 20, which promotes greater adhesive strength between the Cu wirings and the solder balls. Thus, the semiconductor device

experiences less internal exfoliation of the components and operates with a high level of reliability. (See Page 3, lines 15-21; See Page 19, lines 1-4; and lines 15-24; Page 20, lines 10-25; and Page 21, lines 18-28; and Figures 5 and 6).

For at least the reasons outlined above, Applicant respectfully submits that neither the Prior Art nor Lee disclose, teach or suggest all of the features of the independent claim 20.

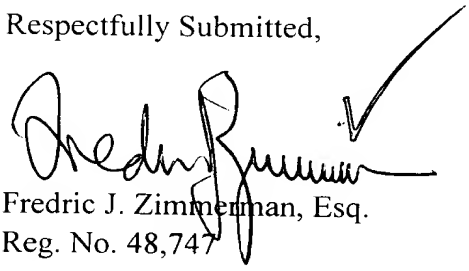
IV. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 1- 4 and 16-23, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,



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